

## ABSTRACT OF THE DISCLOSURE

The present invention provides an error correction circuit for receiving and decoding a trellis-encoded signal of a series of data  $Z_q, Z_{q-1}, \dots, Z_1$  which comprises convolutional-encoded bits and unencoded bits, the convolutional-encoded bits being obtained by convolutional-encoding lower  $t$  bits  $X_t, X_{t-1}, \dots, X_1$  of an input  $p$ -bit series of data  $X_p, X_{p-1}, \dots, X_1$  (where  $p \geq 2$ ,  $q \geq p$ , and  $p > t \geq 1$ ), and the unencoded bits being obtained by not convolutional-encoding upper  $(p-t)$  bits thereof. The circuit includes: a maximum likelihood decoder for preselecting one of  $m$  parallel paths of transition from state  $x$  at time  $k$  to state  $y$  at time  $k+1$ .